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Examiner: PHAM, THANHHA S, Art Unit 2813 Attorney Docket No. 10113171
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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A method of filling a bit line contact via, comprising:
providing a substrate having a device region and periphery region, the device region having a transistor with a gate electrode, drain region, and source region on the substrate;
forming a dielectric layer overlying the substrate, the dielectric layer having a bit line contact via exposing the drain region, and periphery contact via exposing the periphery region;
forming a doped conductive layer, lower than the ~~dielectric layer~~ top surface of the gate electrode, overlying the drain region;
conformally forming a barrier layer overlying the dielectric layer, doped conductive layer, and periphery region; and
forming a first conductive layer filling the bit line contact via and periphery contact via.

Claim 2 (original): The method as claimed in claim 1, wherein the dielectric layer is oxide.

Claim 3 (original): The method as claimed in claim 1, wherein the doped conductive layer is polycrystalline silicon doped with As.

Claim 4 (original): The method as claimed in claim 1, wherein forming the doped conductive layer further comprises:
forming the doped conductive layer overlying the drain region, dielectric layer, and periphery region; and
removing the doped conductive layer by etching, thereby leaving a doped conductive layer overlying the drain region.

Claim 5 (original): The method as claimed in claim 1, wherein the barrier layer prevents the diffusion of the first conductive layer.

Claim 6 (original): The method as claimed in claim 1, wherein the barrier layer comprises a TiN layer.

Claim 7 (original): The method as claimed in claim 1, wherein the first conductive layer is tungsten.

Claim 8 (original): The method as claimed in claim 1, wherein the periphery region is a doped region.

Claim 9 (original): The method as claimed in claim 1, wherein the periphery region is a second conductive layer, and the gate electrode further comprises the second conductive layer.

Claim 10 (original): The method as claimed in claim 9, wherein the second conductive layer is a silicide layer comprising tungsten.

Claim 11 (currently amended): A method of a filling bit line contact via, comprising:
providing a substrate having a device region and periphery region, the device region having a transistor with a gate electrode, drain region, and source region on the substrate;
forming a dielectric layer overlying the substrate, the dielectric layer having a bit line contact via exposing the drain region, and periphery contact via exposing the periphery region;
forming a doped conductive layer overlying the drain region, dielectric layer, and periphery region;
~~removing~~ etching the doped conductive layer ~~using etching, thereby remaining~~ to leave a remaining portion of the doped conductive layer [[,]] lower than the ~~dielectric layer~~ top surface of the gate electrode [[,]] overlying the drain region;
conformally forming a barrier layer overlying the dielectric layer, doped conductive layer, and periphery region; and
forming a first conductive layer filling the bit line contact via and periphery contact via.

Claim 12 (original): The method as claimed in claim 11, wherein the dielectric layer is an oxide layer.

Claim 13 (original): The method as claimed in claim 11, wherein the doped conductive layer is polycrystalline silicon doped with As.

Claim 14 (original): The method as claimed in claim 11, wherein the barrier layer prevents the diffusion of the first conductive layer.

Claim 15 (original): The method as claimed in claim 11, wherein the barrier layer comprises a TiN layer.

Claim 16 (original): The method as claimed in claim 11, wherein the first conductive layer is tungsten.

Claim 17 (original): The method as claimed in claim 11, wherein the periphery region is a doped region.

Claim 18 (original): The method as claimed in claim 11, wherein the periphery region is a second conductive layer, and the gate electrode further comprises the second conductive layer.

Claim 19 (original): The method as claimed in claim 18, wherein the second conductive layer is a silicide layer comprising tungsten.

Claim 20 (new): A method of a filling bit line contact via, comprising:
providing a substrate having a device region and periphery region, the device region having a transistor with a gate electrode, drain region, and source region on the substrate;
forming a dielectric layer overlying the substrate, the dielectric layer having a bit line contact via exposing the drain region, and periphery contact via exposing the periphery region;
conformally forming a doped conductive layer overlying the drain region, dielectric layer, and periphery region;
etching the doped conductive layer to leave a remaining portion of the doped conductive layer lower than the top surface of the gate electrode overlying the drain region;
conformally forming a barrier layer overlying the dielectric layer, doped conductive layer, and periphery region; and

forming a first conductive layer filling the bit line contact via and periphery contact via.